METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN A DIGITAL PROCESSOR

Abstract of the Disclosure

A method and apparatus for reducing power consumption within a pipelined processor. In one embodiment, the method of the invention comprises defining an instruction which invokes a "sleep mode" within the processor and pipeline; inserting the instruction into the pipeline; decoding and executing the instruction, stalling the pipeline in response to the sleep mode instruction; disabling memory in response to the sleep mode instruction; and awaking the core from sleep mode based on the occurrence of a predetermined event. Methods for structuring core pipeline logic and extension instructions to reduce core power consumption under various conditions are described. Methods and apparatus for synthesizing logic implementing the aforementioned methodology are also disclosed.